UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/434,082	11/05/99	RYAN	K 303.306US2

021186 TM02/0327
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH
P.O. BOX 2938
MINNEAPOLIS MN 55402

EXAMINER	
PEIKARI, B	
ART UNIT	**PAPER NUMBER**
2186	6

DATE MAILED: 03/27/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Appl...(s)
09/434,082	Ryan
Examiner	**Group Art Unit**
B. James Peikari	2186

☒ Responsive to communication(s) filed on *Nov 5, 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *5-8 and 29-56* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *5-8 and 29-56* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *3, 4, 5*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Objections

1. Claims 5-8 and 29-56 are objected to because none of the claims gives a clear depiction of the buffering which is being performed in the invention (note Figure 4 of the present application).

All of the claims should be amended to include the language (1) "a data register" and "a command register" or (2) "a data buffer" and "a command buffer" or (3) "a data device for buffering data" and "a command device for buffering commands", as applicant prefers.

While, "instruction" would be more proper, the term "command" has been used throughout the specification and drawings. Some of the present claims include such confusing language as a "buffer register". Note that a register *is* a buffer. These same claims also recite "data register". Other claims recite "data devices" and "buffer devices" which would normally appear to mean the same thing. For clarity, the claims should be amended as suggested above.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5-8 and 29-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al., U.S. 5,875,452, in view of Sakakibara et al., U.S. 5,617,575.

Katayama et al. teach the claimed invention in a memory system comprising a memory controller (*note memory controller 17*) with a unidirectional command and address bus (*note that both the ROW-Add and COL-Add lines of the address bus are unidirectional, further, all command inputs to clock generator 30 are unidirectional*), a bidirectional data bus (*note that data I/O is bidirectional*), a plurality of memory devices (*note the use of two exemplary DRAM devices 22*), a buffer register coupled between the command and address bus and the plurality of memory devices for receiving and latching commands and addresses (*note the combination of column address buffers 34 and 44 and row address buffers 32 and 36; note also columns 17-18, which state, "The row decode buffer 36 corresponds to an address buffer ... The column decode buffer 44 also corresponds to the address buffer"*), a data register connected between the plurality of memory devices and the bidirectional data bus for receiving and latching read data or write data (*note the combination of read buffer 54 and write buffer 52, note also column 18, which states, "The read buffer 54 and the write buffer 52 correspond to a data buffer according to this invention, and are connected to the data bus"*). As for the claimed pipelined packet protocol, including the first and second delays, note that buffers and registers *always* introduce delays by their very nature, and the use of delays (or wait states) was critical to the operation of any pipelined data processing system. Note also column 2, lines 34 et seq. and column 20, line 6.

As for the feature of *each* memory device containing a data in and a data out buffer, a column decoder and a row decoder, it was noted in St. Regis Paper Co. v Bemis Co. 193 USPQ 8 (7th Cir. 1977) that to duplicate parts for multiple effects is *not* given patentable weight. In any case, Figure 9 shows an embodiment of the Katayama et al. system which clearly displays dedicated row and column decoder circuitry for each of the plurality of memory devices 22. In fact, it is clear from the description that each of the devices 22 in Figure 2 have similar dedicated circuitry, although this was not shown in the drawing. Further, the plurality of groups of sense amps 28 (note column 17, lines 12-14) in Figure 2 would have required multiple dedicated read and write buffers 54 and 52.

While Katayama et al. teaches most of the features of the invention as described above, there is no specific teaching of a shared command buffer and a shared data buffer, where these buffers are shared among plural memory banks. However, shared buffers were well known in the prior art. In fact, as stated in the previous advisory action, most of the present claims are written so broadly that they would have been taught by the use of an instruction buffer and data buffer at the processor (12) of the Katayama et al. system.

Although Katayama et al. did not discuss the structure of the processor (12), it is noted that most processors on the market at the time of the invention utilized integral data buffers and instruction buffers at the respective bus interfaces.

In any case, Sakakibara et al. has been cited as an example of this well known use of shared command and data buffers, since the drawings more plainly demonstrate this feature

(compare Figure 1 of Sakakibara et al. to Figure 4 of the present invention). Note that Sakakibara et al. teaches a shared command buffer unit, SCU 9, which contains buffers in the queues and transmits commands for the connectivity to the memory banks, as well as a shared data buffer unit 23.

It would have been obvious to include the DRAM banks of Katayama et al., with all of their peripheral circuitry, as the banks in the Sakakibara et al. system of shared buffers, since (1) memory "banks" were often DRAM arrays and (2) the uniform access times provided by the Katayama et al. system would have provided more streamlined performance, especially in the highly parallel environment of the Sakakibara et al. system.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 5-8 and 29-56 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4, 26-28 and 32-57 of copending Application No. 08/886,753. Although the conflicting claims are not identical, they are not patentably distinct from each other because each and all of the features of the present claims are included in the claims of the '753 application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Although the present application is a divisional of the '753 application, and the divisional resulted from a restriction requirement,

(1) the examiner concedes that claims 26-28 should have been included in group II, as opposed to group I. However,

(2) it is noted that *after* the restriction requirement was made, applicant never amended the claims 26-28 to be consonant with the restriction requirement;

quite the contrary,

(3) applicant added *more* claims directed to pipelining to the '753 *and*

(4) added several claims (specifically 38-43) to the present application which do not even mention pipelining at all.

Thus, both applications have been amended such that there is no longer any patentable distinction between the two sets of claims. Thus, a provisional obviousness-type double patenting rejection is deemed proper.

The following are situations where the prohibition of double patenting rejections under 35 U.S.C. 121 does not apply: .....

(b) The claims of the different applications or patents are not consonant with the restriction requirement made by the examiner, since the claims have been changed in material respects from the claims at the time the requirement was made. For example, the divisional application filed includes additional claims not consonant in scope to the original claims subject to restriction in the parent. Symbol Technologies, Inc. v. Opticon, Inc. , 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991); Gerber Garment Technology, Inc. v . Lectra Systems Inc. , 916 F.2d 683, 16 USPQ2d 1436 (Fed. Cir. 1990).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (703) 305-3824.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051 (for formal communications intended for entry)

or:

(703) 305-9731 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

B. James Peikari
Primary Examiner
Art Unit 2186

March 24, 2001